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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/709,695	11/10/2000	Richard Anthony Ferreri	10007479-1	4628

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EXAMINED

PALADINI, ALBERT WILLIAM

ART UNIT	PAPER NUMBER
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2125

DATE MAILED: 02/23/2004

5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/709,695	FERRERI ET AL.	
	Examiner	Art Unit	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>4</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1

Line 2 recites "one cell that describes a device," and lines 3-4 recite, "where the instances describe devices that are used to form the functionality of the cell." If the function of the cell is to describe a single device in the system as recited in line 2, it is not understood what "devices that are used to form the functionality of the cell" means. This refers to plural devices related to a cell.

Claim 4

The term "O (log N)" is not understood.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art.

This rejection is made to the extent that the claims are understood.

Referring to figure 1, Applicant states on lines 6-7 on page 2, "Such a configuration is known as a folded connectivity model. The cell block 101 describes a device or structure of the system." Applicant states on lines 14-16 on page 2, "In this way a design hierarchy can be created. The instance block describes the devices or structures used to form the functionality of a cell." Applicant states on lines 20-21 on page 2, "The hierarchical nature of the information stored in the folded connectivity

model is shown by way of example only in FIGURES 2A-2C.” Applicant states on lines 10-13 on page 4 “For these reasons, the occurrence (or unfolded) model representation is becoming a more important representation for many of today’s CAD tools. FIGURE 9 represents a typical occurrence model. In an occurrence model, each and every cell is stored, including those cells that are duplicated, while retaining the notion of the original design hierarchy.”

Thus, the Applicant’s admitted prior art depicted in figures 1, 2, and 9 teaches a cell that describes a device within a system, defining instances of the cell used to form the functionality of the cell, utilization of a folded connectivity model an occurrence model. The Applicant does not explicitly describe “occurrence nodes” as recited in claim 1 and its dependent claims and pointers of the occurrence nodes as recited in claims 11, 16, and many of their dependent claims.

However, it would have been obvious to one of ordinary skill in the art that the “occurrence model” depicted in figure 9 and described on lines 10-19 on page 4 must contain “occurrence nodes” and “pointers.”

Relevant Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dangelo (5870308) discloses a hierarchical knowledge base approach to simulate hardware descriptions in a high-level Hardware Description Language (HDL). In this approach, a

knowledge base is constructed corresponding to each functional block of the hardware description. The hierarchical relationships among the various blocks in the description are mapped on to the knowledge base corresponding to those blocks. The hierarchical knowledge base thus formed is used for simulating the hardware description. Unlike previous approaches to simulation and verification of digital circuits (devices) described in a HDL, there is no need for intermediate translation steps.

Bentley (6063128) discloses an object –oriented computer modeling system designed to construct a model from component objects, which can be recalled, updated and saved on a continuous basis.

Kant (6173276) discloses a software system capable of solving partial differential equations, which creates a software problem-solving environment ("PSE") for automatically transforming a mathematical modeling problem specification into an executable numerical program. The System's close integration with a computer algebra system confers more powerful code generation abilities than libraries or conventional expert systems. The System can be thought of as a very smart optimizing compiler, with optional directives, for a language consisting of mathematical and application specific terms. To minimize the information-correctness problem, the System maximizes the recording of information in machine manipulatable form. The information is kept as a network of small chunks with well-defined relationships. An object instance or attribute or a specification file represents a node of the network. The relationships among nodes are: definition/short description, examples, syntax, longer narrative description, related node, alternative node.

Singh (6539536) discloses a design automation system which includes a computer implemented process and system for electronic design automation (EDA) using groups

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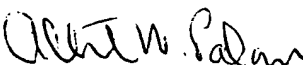
of multiple cells having loop-back connections for modeling port electrical characteristics. Multi-bit cells have multiple gates of the same function implemented within a same cell. Multi-bit components have multiple multi-bit cells implemented within a same component.

7. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (703) 308-2005. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (703) 308-0538. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

February 19, 2004


Albert W. Paladini
Primary Examiner
Art Unit 2125